Remarks

These remarks are in response to the second non-final substantive Office Action of June 1, 2006, for which a one-month extension is hereby requested. The Office Action rejected all of the pending claims under 35 USC 103, with some claims additionally rejected under 35 USC 112, second paragraph, and other claims being objected to on various bases. The claims have been amended as indicated above due to the objections and some of the rejections under 35 USC 112, second paragraph. It is believed that the rejections under 35 USC 103 are not well founded and should be with drawn. These are all discussed below under the corresponding headings.

Claim Objections

The Office Action objected to a number of claims. The various objections raised in the Office Action have been attended to as indicated above in the listing of claims, with claim 91 being rewritten in independent form and new claims 105-110 having been added due to the objection at paragraph 6.

Rejections under 35 USC § 112

The Office Action rejected a number of claims under 35 USC 112, second paragraph. Aside from the rejections at paragraphs 21-23 and 27, these have been attended to as indicated above in the listing of the claims. With respect to paragraph 21, the antecedent for "the intermediate circuit stress time value" in lines 10-13 of claim 64 is "an intermediate circuit stress time value" at lines 7-8. With respect to paragraph 22, the antecedent for "the non-aged version" in line 6 of 76 is "a non-aged version" in lines 3-4. With respect to paragraph 23, the first element of claim 76 is "revising the netlist, ...", providing the antecedent for "the revised netlist" in line 10. With respect to paragraph 27, it is unclear where "the magnitude" is found in line 2 of claim 95.

Rejections under 35 USC § 103

The Office Action rejected claims 1-7, 9-20, 22-39, 52-58, 61-65, 76, 77, 91, are 92-104 under 35 USC 103(a) as being unpatentable over Kadoch et al. (US patent 5,761,481) in view of Rajgopal et al. (US patent 6,363,515) and further in view of Chen et al., "A Unified Compact

Scalable Model for Hot Carrier Reliability Simulation". It is respectfully submitted that these rejections are in error.

Claims 1-7

Claim 1 is drawn to an aspect of the present invention that allows for simulating for multiple stress time values in a single run, as is described, for example, beginning on line 7 of page 8 of the present application. It is respectfully submitted that such a method is neither taught nor suggested by Kadoch, Rajgopal, or Chen, either alone or in combination. In its rejection of claim 1, the Office Action relies upon Chen for the majority of claim elements, with Rajgopal cited for the netlist and the netlist's specification of components. Kadoch is cited as the primary reference, but is cited only at column 2, line 62, and only for the "simulating in a single run" limitation. The Office Action is correct in that neither Rajgopal nor Chen allow for simulating for multiple stress time values in a single run. Kadoch does discuss a single run of a simulator to cover several cases; however, what Kadoch is doing is very specific. It is respectfully submitted that what Kadoch presents does not disclose, and does not suggest anything that would render as obvious, simulating a circuit for multiple stress time values in a single run to determine its degraded operation.

Kadoch teachings are all directed at experimental N-channel transistor modeling. The simulations described are all for the modeling of a *single device* to optimize the manufacturing process. In contrast, the claims of the present application are all drawn to the simulating of *circuit* operation, whereas Kadoch is only concerned with a single device. Consequently, although the Office Action lists Kadoch as the primary reference, it only concerned with single devices of a specific type, rather than circuits.

Kadoch does describe a process simulator to produce simulations of structures of varying channel lengths in a single run, but the processes are quite specific and particular to channel length: its look at half of a transistor, models what is going on for this half structure, then adapts it for one of multiple channel lengths and performs a simulation on the whole device structure. As can be seen by looking, for example, at Kadoch's Figure 5 and its explanation, the techniques being used are very much tied to transistor structure, channel length, and properties dependent upon transistor length. What Kadoch presents does not concern time values and aging and it is

unclear how these would be adapted, or even if they could be adapted, to time and device degradation of a single device, much less an entire circuit. To use such teaching for circuit degradation simulation for multiple time values would, at best, be based on hindsight gained from the present application, which is improper. Further, even with such improper hindsight, it is unclear how such teaching for a single device and for multiple channel length would be adapted as suggested in the Office Action.

Further, even for a channel length and for a single device, what Kadoch is presenting does not determine device operation for multiple channel lengths in a single simulation. Rather, although the early stages of the process are not for a specific channel length, Kadoch requires that the actual channel length is put in before device simulations are performed on the full structure. Consequently, before the end result, it needs to have specified a single value for the channel length. It is only the early portions of Kadoch's process that are not length specific. This can be seen by looking at the Summary at column 2, lines 40-60, or referring again to Kadoch's Figure 5: note that step 512 in the middle of the flow requires a specific channel length be prescribed before continuing on to step 514 to finish simulating the device.

More specifically, claim 1 has as its second element:

> supplying a plurality of circuit stress time values;

and ends with

> determining degraded operation of the circuit by *simulating in a single run operation of the circuit* with the specified components using their respective aging model information and respective relative component degradation parameter *at the plurality of supplied circuit stress time values*.

The emphasis has been added. For the "simulating in a single run operation of the circuit", the Office Action cites Kadoch at column 2, line 62, which refers to "a single run of a process simulator to produce simulations of structures of varying channel lengths". However, as discussed above, Kadoch's teachings are all directed to simulation of a *single device*, not a circuit of multiple components; are quite specific and tied to variations is channel length, so that it is unclear how, or even if, these would relate to the degradation level at differing time values; and it is only the early stages of Kadoch's simulation process that is for multiple channel length, as a prescribed channel must be input at an intermediate stage before the simulation can be completed.

Therefore, for at least these reasons, it is respectfully submitted that a rejection of claim 1, along with its dependent claims (2-7, 9-20, 22-39, 52-58, 61-65, 76, 77, and 93-98), under 35 USC 103(a) as being unpatentable over Kadoch in view of Rajgopal and further in view of Chen is in error and should be withdrawn.

A number of these dependent claims are believed further allowable for their additional limitations. For example, claim 4 includes the further limitation of "wherein the simulating is performed using a timing simulation type circuit simulator", for which the Office Action cites Chen at page 246, figure 5, "stress time"; however, this only refers to how long the circuit has been stressed and has no reference to a timing simulation type of simulator (such as Starsim or Timemill, as opposed to a SPICE type simulator, examples being as HSPICE or Spectre). Chen does refer to SPICE modeling technology, but does not appear to disclose a timing simulation type of circuit simulator. Consequently, claim 4 is believed further allowable on this basis.

As for claim 5, this includes the further limitation of "wherein the aging model information on the selected ones of the components is derived from electrical test data." The Office Action cites Chen for the "aging model" and Rajgopal for "selected ... components", but supplies no citation for "derived from electrical test data", which is the substance of the limitation. Consequently, the rejection is improper and claim 4 is believed further allowable on this basis.

Similarly, claim 7 includes the further limitation of "wherein determining the degraded operation of the circuit comprises determining the circuit's speed at the supplied circuit age parameters", for which the Office Action cites Chen at page 244, equation 2 with right column, lines 4-8. The cited location does refer to age, but there is no disclosure of circuit speed and, in particular, of "determining the circuit's speed".

Concerning claim 6, this contains the limitation that "said simulating the behavior of the fresh circuit" from claim 1 "determines the waveforms at the nodes to which the selected ones of the components are connected relative to an input waveform." For this additional element, the Office Action refers to Chen's figure 10, the "Fresh" curve; however, Chen's figure 10 does not show waveforms at a node relative to an input waveform or anything else, but just presents I-V curves for a fresh device and then a stressed device for a number of different gate voltages.

Claims 93 and 9-20

Claim 93 depends upon claim 1 and is believed allowable on this basis alone. Claim 93 is further drawn to an aspect of the present invention allowing different performance criteria to be applied to different circuit blocks. This is described in the paragraph beginning on page 8 at line 20. In particular, claim 93 includes:

> supplying an independent performance criterion for each set of said plurality of distinct sets of components;

for which the Office Action cites Rajgopal at column 8, lines 40-42. The cited portion of Rajgopal is a claim: "The method of claim 7 including the power use of the system that includes components and the power use of said components." This neither teaches nor suggests "supplying an *independent performance criterion* for *each set* of said plurality of distinct sets of components".

Further, the next element of claim 93 is:

> wherein said supplying aging model information includes supplying aging model information on selected components from each of said sets of components,

for which the Office Action provides no citation in any of the references and which is not believed to be found in the cited references. (In its rejection of claim 93, the Office Action does not include this element when it lists the claim.)

Consequently, for any of these reasons, a rejection of claim 93, along with its dependent claims 9-20, under USC 103(a) as being unpatentable over Kadoch in view of Rajgopal and further in view of Chen is believed to be further in error on this basis.

A number of claims 9-20 are believed further allowable for their additional limitations. Concerning claims 9-20, for "distinct sets of components", the Office Action again refers to Rajgopal at column 8, lines 40-42, which was quoted above. This passage has no disclosure of "distinct sets of components", only "the system" and "components" it contains. This passage is also cited for "an analog block" and "a digital block", which are also not found there. As to the specifics of the various claims, in claim 12, for example, the Office Action provides a list of components without providing a citation for them. Concerning claim 15, the cited location of Chen does describe "forward/reverse operation", but not "driving capability" or a "performance criterion" therefor, which is what is recited in the claim. Concerning claim 16, the Office Action states "JFETs well-known", which may be true; but the claim recites "bipolar junction

transistor", which a JFET is not, being instead a field effect transistor. Concerning claim 18, the Office Action provides no citation for "different models for simulating the same device type."

Claims 94 and 22-39

Claim 94 depends upon claim 1 and is believed allowable on this basis alone. It is believed further allowable as it also drawn to the aspect of the present invention presented whereby the depredation level of selected components can be specified, as opposed to determining the level of degradation for other elements. This is described, for example, beginning on page 9, line 20, of the present application as part of optional step 103 in Figure 5. In particular, claim 94 includes the additional element of:

> specifying the degradation level of a second set of selected components of the circuit, wherein the elements of the first set and the second set of components are distinct,

where the degraded operation of the circuit then uses these specified values for the selected set of components, while the other set of components again uses the determined level of degradation. For this limitation, the Office Action again cites Rajgopal, column 8, lines 40-42: "The method of claim 7 including the power use of the system that includes components and the power use of said components." This passage does not disclose either the use of a degradation level or its specification. Neither in this cited portion nor, as far as can be determined, elsewhere in Rajgopal is there any teaching or suggestion of "specifying the degradation level of a second set of selected components of the circuit". Consequently, a rejection of claim 94, along with its dependent claims 22-39, under 35 USC 103(a) as being unpatentable over Kadoch in view of Rajgopal and further in view of Chen is believed to be further in error on this basis.

Dependent claims 22-36 are drawn to various examples of what the "first set" and "second set" of components may be, and to various examples of how the degradation level may be specified. As with claims 9-20, the Office Action again cites Rajgopal, column 8, lines 40-42, for the division of components into a first and second set. As already discussed, it is again respectfully submitted that is in error. A number of claims 22-36 also believed further allowable for the additional limitations they contain. For example, claims 23 and 25 recite that the "second set of components form", respectively, "a digital block" and "an analog block", for both of which the Office Action again cites Rajgopal, column 8, lines 40-42, when neither of these are found

there. For claims 31, 32, 34, and 35, see the remarks above concerning claims 15, 16, 18, and 19, respectively.

Concerning claims 37 and 39, these give specific examples of ways of specifying the level of degradation. In claim 37, "the degradation level of the second set of selected components is specified as a relative component degradation parameter with respect to the component degradation parameter of the first set of components", for which the Office Action cites Chen at page 243, left column, line 6. It is respectively submitted that the use of such a relative scale of degradation is not found in Chen at this location or, as far as can be determined, elsewhere in the cited references. In claim 39, "the degradation level of the second set of selected components is expressed in terms of lifetime", for which the Office Action cites "Chen: pg. 244, line 7", presumably the right column; however, this just states that H and m are lifetime parameters. Consequently, claims 37 and 39 are believed further allowable on this basis.

Claims 95, 96 and 52-58

Claim 95 depends upon claim 1 and is again believed allowable on this basis alone. Claim 95 is further drawn to an aspect of the present invention where multiple current sources are added to represent different degradation mechanisms, as shown in Figure 6 of the present application and described beginning on page 13, line 4, with more detail given starting in the paragraph beginning on line 17 of that page. In particular, claim 95 includes:

> revising the netlist, wherein ***each*** *of said selected components is replaced by a non-aged version of the selected component and a* ***plurality of independent current sources*** *corresponding to different mechanisms connected between the terminals of the non-aged version*, wherein a magnitude of a current relative to a circuit stress time in each of the current sources of a component is determined from the aging model information of the component and a ***distinct*** *mechanism degradation parameter* derived from the component degradation parameter; and
>
> wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with the revised netlist at the supplied circuit stress time values.

The emphases have been added to highlight those elements that particularly distinguish this claim. For "revising the netlist", the Office Action cites Rajgopal at column 5, line 63: this describes a mapped netlist, but not its revision. Continuing on to the elements emphasized in the claim, for "wherein ***each*** *of said selected components is replaced by a non-aged version of the selected component*" the Office Action cites Rajgopal at column 8, lines 40-42; however, this has

no disclosure of "a non-aged version" of a component (or aging at all), no disclosure of replacing components, and specifically no disclosure "selected components [being] replaced by a non-aged version of the selected component".

For the "a plurality of independent current sources corresponding to different mechanisms connected between the terminals of the non-aged version", the Office Action refers to "'Fresh' Chen, pg.247, figure 11). Figure 11 of Chen shows a simulation for a ring oscillator that includes a trace for a fresh model, but it is unclear what is the relation to the claim element: There is nothing related to current sources, specifically not a *plurality* of *independent* current sources connected as in the claim. For "a distinct mechanism degradation parameter", the Office Action cites Chen at page 243, left column, second paragraph, line 6: this only has general mention of "degraded device characteristics", not "a distinct mechanism degradation parameter" to determine the "magnitude of the current ... in each of the current sources".

Consequently, for at least these reasons, a rejection of claim 95, along with its dependent claims 96 and 52-58, under 35 USC 103(a) as being unpatentable over Kadoch in view of Rajgopal and further in view of Chen is believed to be further in error on this basis.

Concerning claim 96, this further incorporates an aspect of the present invention allowing for device models to be updated. This aspect is discussed below with respect to claim 97 and the Examiner is referred to the first paragraph under the next heading. Claim 96 is further believed allowable on this basis.

Concerning claim 55, this claim further includes "determining a magnitude of a respective current in each of the independent current sources", where said determining includes "supplying a physical model of the current magnitude" and "establishing values of coefficients in the physical model from electrical test data". For "establishing values of coefficients", the Office Action refers to Chen's equation 7; however the coefficients given there are just described as fitting parameters and no disclosure is given of them being established from electrical test data. Additionally, the model presented in this section of Chen is not for the magnitude of a current source, but for current degradation, where Chen's figure 5 looks at the model for various stress times.

Concerning claims 56, this includes the limitation that the degradation level of selected components is expressed in terms of lifetime. As discussed above with respect to claim 39, the cited location of Chen just states that *H* and *m* are lifetime parameters.

Claim 58 includes that the revising of the netlist is embedded in the circuit simulator. The Office Action refers to Rajgopal at column 5, line 63; however, this only discloses a mapped netlist, which has no such embedding of netlist revisions. Thus, claim 65 is believed further allowable on this basis.

Claims 97 and 61-65

Claim 97 depends upon claim 1 and is again believed allowable on this basis alone. Claim 97 is further drawn to an aspect of the present invention allowing for device models to be updated, as described, for example, beginning on page 15, line 18, of the present application, and is believed further allowable on this basis. In particular, the simulating of claim 97 "includes incorporating aging of the selected components by updating the models of said circuit simulator". The Office Action again cites Rajgopal at column 8, lines 40-42: "The method of claim 7 including the power use of the system that includes components and the power use of said components." This does not disclose the use of models, updating of models, or incorporating aging. Neither in this location nor, it appears, elsewhere in the cited references is the updating of a circuit simulator's models described. In particular, Rajgopal does not "incorporat[e] the aging of the selected components" by such an updating. Consequently, a rejection of claim 97, along with its dependent claims 61-65, under 35 USC 103(a) as being unpatentable over Kadoch in view of Rajgopal and further in view of Chen is believed to be further in error on this basis.

Concerning claims 62 and 63, these respectively include the limitation that "incorporating the aging of the selected components comprises including the time dependence of a substrate current", and "a gate current", respectively. With respect to the "substrate current", the Office Action provides no citation for this element, only the previously used citation for "selected components". With respect to the "gate current", the Office Action cites Chen on page 244, right column "Gate bias dependency"; however, this section concerns the gate bias dependency of the

source to drain current and does not relate to "a gate current" or its time dependence. Thus, claims 62 and 63 are believed further allowable on this basis.

As for claim 64, this further includes the sub-aspect of "gradual aging", described in the paragraphs beginning on page 15, line 7, of the present application. Claim 64 includes determining an "intermediate component degradation parameter" on selected components by simulating the fresh behavior of the circuit, for which the Office Action cites Chen at page 243, left column, second paragraph, lines 9-10. It is respectfully submitted that this cited location only contains some general comments on and that there is no discussion of determining "intermediate component degradation parameters". Thus, claim 64 is believed further allowable on this basis.

Claim 65 includes that the updating of models is embedded in the circuit simulator, similar to the aspect discussed above with respect to claim 58 for revising the netlist. The Office Action provides no citation for "updating the models of said circuit simulator is embedded in the circuit simulator", only again referring to Rajgopal claim 7 for "selected components". Thus, claim 65 is believed further allowable on this basis.

Claims 98, 76, and 77

Claim 98 depends upon claim 1 and is again believed allowable on this basis alone. It is believed further allowable as it also is drawn to the "quantizing" aspect of the present invention presented, for example, beginning on page 14, line 9, of the present application. In particular, claim 98 includes:

quantizing each of said relative degradation levels to one of a plurality of discrete values;

and then using the quantized relative degradation levels at the supplied circuit stress time values. The Office Action cites Chen at page 246, equation 7 with line 1; however, this is an equation for the length of a damaged channel region and line 1 just states that elements in this equation are fitting parameters. Neither in the cited location nor, as far as can be determined, elsewhere do the references teach or even disclose such quantizing of relative degradation levels. Consequently, a rejection of claim 98, along with its dependent claims 76 and 77, under 35 USC 103(a) as being unpatentable over Kadoch in view of Rajgopal and further in view of Chen is believed to be further in error on this basis.

Claim 76 further introduces revising the netlist, as discussed above with respect to claim 95, and thus believed further allowable on this basis.

Claim 77 includes that the quantization is embedded in the circuit simulator, similar to the aspect discussed above with respect to claim 58 for revising the netlist, and thus believed further allowable on this basis.

Claims 91, 92, 99-104 and new claims 105-110

Claim 91 incorporates the limitations of claim 1. Claims 105-110 depend upon the claim 91 and further incorporate the limitations of claim 93-98. Consequently, each of claims 91 and 105-110 is believed allowable for the reasons given above for claims 1 and 93-98, respectively.

Similarly, claim 92 incorporates the limitations of claim 1. Claims 99-104 depend upon the claim 92 and further incorporate the limitations of claim 93-98. Consequently, each of claims 92 and 99-104 is believed allowable for the reasons given above for claims 1 and 93-98, respectively.

Information Disclosure Statement

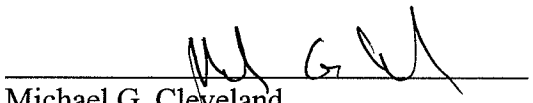
Another copy of the Leblebici et al. reference that the Office Action noted as illegible is being submitted.

Conclusion

For the reasons given above, it is believed that the pending claims are allowable. Reconsideration of claims 1-7, 9-20, 22-39, 52-58, 61-65, 76, 77, and 91-104, and consideration

of new claims 105-110, is respectfully requested and an early indication of their allowability is earnestly solicited.

Respectfully submitted,



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